

NLAST44599

Low Voltage Single Supply Dual DPDT Analog Switch

The NLAST44599 is an advanced CMOS dual-independent DPDT (double pole-double throw) analog switch, fabricated with silicon gate CMOS technology. It achieves high-speed propagation delays and low ON resistances while maintaining CMOS low-power dissipation. This DPDT controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The device has been designed so the ON resistance (R_{ON}) is much lower and more linear over input voltage than R_{ON} of typical CMOS analog switches.

The channel-select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The NLAST44599 can also be used as a quad 2-to-1 multiplexer-demultiplexer analog switch with two Select pins that each controls two multiplexer-demultiplexers.

- Select Pins Compatible with TTL Levels
- Channel Select Input Overvoltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation: $I_{CC} = 2 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch-up Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V;
Machine Model > 200 V
- Chip Complexity: 158 FETs
- Pb-Free Packages are Available



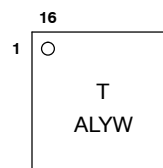
ON Semiconductor®

<http://onsemi.com>

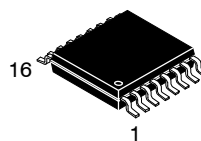
MARKING DIAGRAMS



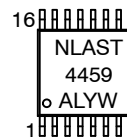
QFN-16
MN SUFFIX
CASE 485G



(TOP VIEW)



TSSOP-16
DT SUFFIX
CASE 948F

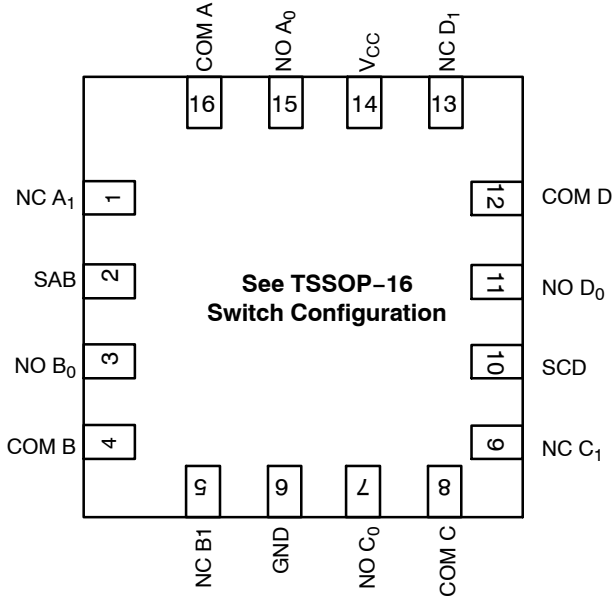


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

QFN-16 PACKAGE



FUNCTION TABLE

Select AB or CD	ON Channel
L	NC to COM
H	NO to COM

TSSOP-16 PACKAGE

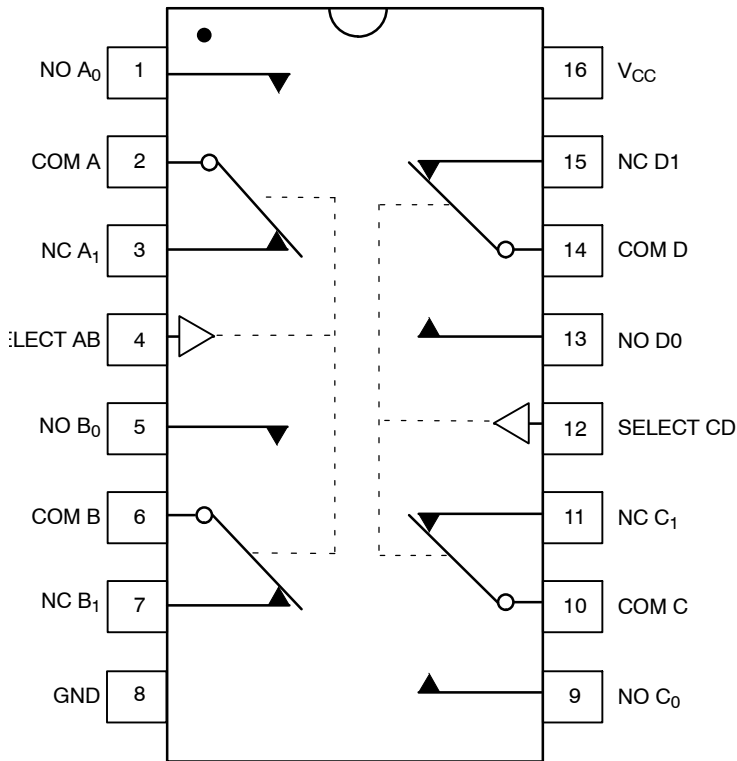


Figure 1. Logic Diagram

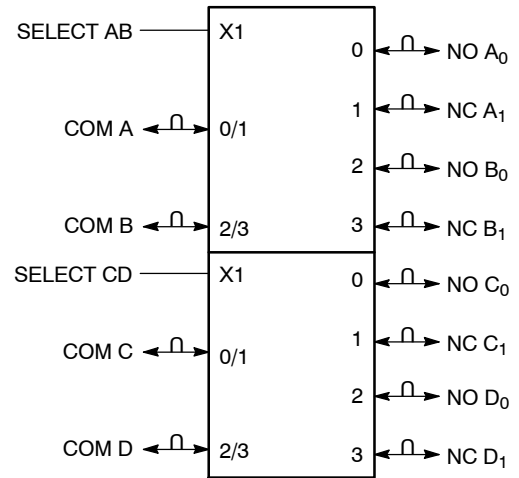


Figure 2. IEC Logic Symbol

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	Positive DC Supply Voltage	- 0.5 to + 7.0	V	
V _{IS}	Analog Input Voltage (V _{NO} or V _{COM})	- 0.5 ≤ V _{IS} ≤ V _{CC} + 0.5	V	
V _{IN}	Digital Select Input Voltage	- 0.5 ≤ V _I ≤ + 7.0	V	
I _{IK}	DC Current, Into or Out of Any Pin	± 50	mA	
P _D	Power Dissipation in Still Air	QFN-16 TSSOP-16	800 450	mW
T _{STG}	Storage Temperature Range	- 65 to + 150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C	
T _J	Junction Temperature Under Bias	+150	°C	
MSL	Moisture Sensitivity	Level 1		
F _R	Flammability Rating	Oxygen Index: 30% - 35%	UL-94-V0 (0.125 in)	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	2000 200 1000	V
I _{LATCH-UP}	Latch-Up Performance	Above V _{CC} and Below GND at 125°C (Note 4)	± 300	mA
θ _{JA}	Thermal Resistance	QFN-16 TSSOP-16	80 164	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	Digital Select Input Voltage	GND	5.5	V
V _{IS}	Analog Input Voltage (NC, NO, COM)	GND	V _{CC}	V
T _A	Operating Temperature Range	- 55	+ 125	°C
t _r , t _f	Input Rise or Fall Time, SELECT	V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 100	ns/V
			20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

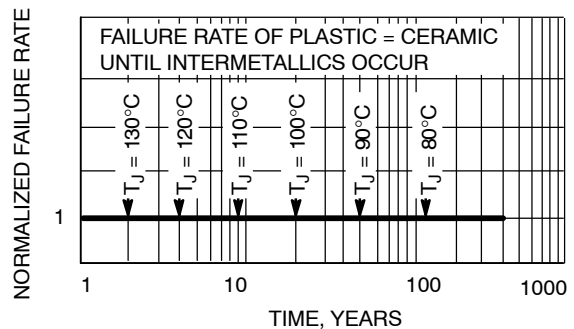


Figure 3. Failure Rate vs. Time Junction Temperature

NLAST44599

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit			Unit
				–55°C to 25°C	< 85°C	< 125°C	
V _{IH}	Minimum High-Level Input Voltage, Select Inputs		3.0	2.0	2.0	2.0	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage, Select Inputs		3.0	0.5	0.5	0.5	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	5.5	± 0.2	± 2.0	± 2.0	μA
I _{OFF}	Power Off Leakage Current, Select Inputs	V _{IN} = 5.5 V or GND	0	± 10	± 10	± 10	μA
I _{CC}	Maximum Quiescent Supply Current	Select and V _{IS} = V _{CC} or GND	5.5	4.0	4.0	8.0	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit			Unit
				–55°C to 25°C	< 85°C	< 125°C	
R _{ON}	Maximum “ON” Resistance (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} V _{IS} = GND to V _{CC} I _{IN} ≤ 10.0 mA	2.5	85	95	105	Ω
			3.0	45	50	55	
			4.5	30	35	40	
			5.5	25	30	35	
R _{FLAT (ON)}	ON Resistance Flatness (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{IS} = 1 V, 2 V, 3.5 V	4.5	4	4	5	Ω
I _{NC(OFF)} I _{NO(OFF)}	NO or NC Off Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 1.0 V _{COM} 4.5 V	5.5	1	10	100	nA
I _{COM(ON)}	COM ON Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{NO} 1.0 V or 4.5 V with V _{NC} floating or V _{NO} 1.0 V or 4.5 V with V _{NO} floating V _{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

NLAST44599

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V _{CC} (V)	V _{IS} (V)	Guaranteed Maximum Limit						Unit	
					-55°C to 25°C			< 85°C		< 125°C		
					Min	Typ*	Max	Min	Max	Min		Max
t _{ON}	Turn-On Time (Figures 12 and 13)	R _L = 300 Ω, C _L = 35 pF (Figures 5 and 6)	2.5	2.0	5	23	35	5	38	5	41	ns
			3.0	2.0	5	16	24	5	27	5	30	
			4.5	3.0	2	11	16	2	19	2	22	
			5.5	3.0	2	9	14	2	17	2	20	
t _{OFF}	Turn-Off Time (Figures 12 and 13)	R _L = 300 Ω, C _L = 35 pF (Figures 5 and 6)	2.5	2.0	1	7	12	1	15	1	18	ns
			3.0	2.0	1	5	10	1	13	1	16	
			4.5	3.0	1	4	6	1	9	1	12	
			5.5	3.0	1	3	5	1	8	1	11	
t _{BBM}	Minimum Break-Before-Make Time	V _{IS} = 3.0 V (Figure 4) R _L = 300 Ω, C _L = 35 pF	2.5	2.0	1	12		1		1		ns
			3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		

*Typical Characteristics are at 25°C.

Symbol	Parameter	Typical @ 25, V _{CC} = 5.0 V		Unit
		Min	Max	
C _{IN}	Maximum Input Capacitance, Select Input		8	pF
C _{NO} or C _{NC}	Analog I/O (Switch Off)		10	
C _{COM}	Common I/O (Switch Off)		10	
C _(ON)	Feedthrough (Switch On)		20	

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V _{CC} V	Typical	Unit
				25°C	
BW	Maximum On-Channel -3 dB Bandwidth or Minimum Frequency Response (Figure 11)	V _{IN} = 0 dBm V _{IN} centered between V _{CC} and GND (Figure 7)	3.0	145	MHz
			4.5	170	
			5.5	175	
V _{ONL}	Maximum Feedthrough On Loss	V _{IN} = 0 dBm @ 100 kHz to 50 MHz V _{IN} centered between V _{CC} and GND (Figure 7)	3.0	-3	dB
			4.5	-3	
			5.5	-3	
V _{ISO}	Off-Channel Isolation (Figure 10)	f = 100 kHz; V _{IS} = 1 V RMS V _{IN} centered between V _{CC} and GND (Figure 7)	3.0	-93	dB
			4.5	-93	
			5.5	-93	
Q	Charge Injection Select Input to Common I/O (Figure 15)	V _{IN} = V _{CC} to GND, F _{IS} = 20 kHz t _r = t _f = 3 ns R _{IS} = 0 Ω, C _L = 1000 pF Q = C _L * ΔV _{OUT} (Figure 8)	3.0	1.5	pC
			5.5	3.0	
THD	Total Harmonic Distortion THD + Noise (Figure 14)	F _{IS} = 20 Hz to 100 kHz, R _L = R _{gen} = 600 Ω, C _L = 50 pF V _{IS} = 5.0 V _{PP} sine wave	5.5	0.1	%
VCT	Channel to Channel Crosstalk	f = 100 kHz; V _{IS} = 1 V RMS V _{IN} centered between V _{CC} and GND (Figure 7)	5.5	-90	dB
			3.0	-90	

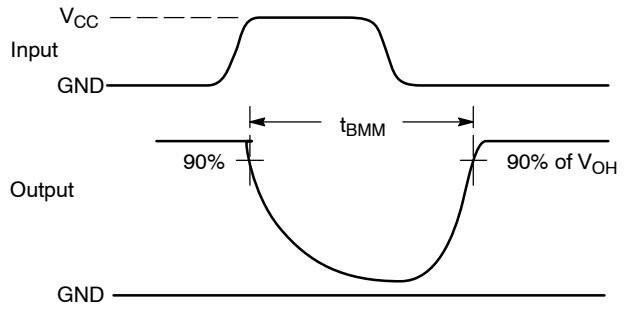
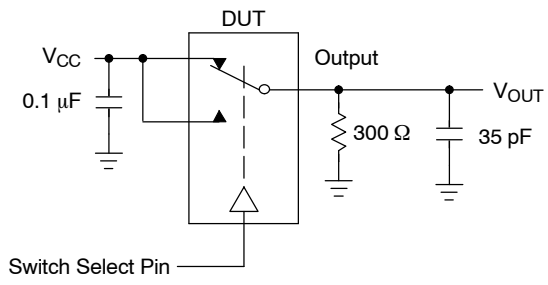


Figure 4. t_{BMM} (Time Break-Before-Make)

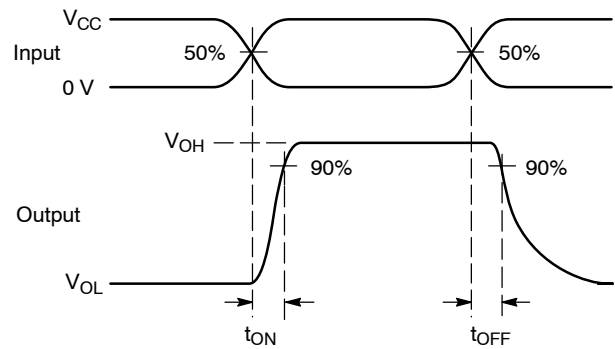
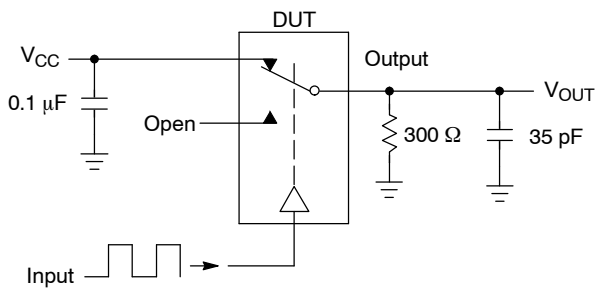


Figure 5. t_{ON}/t_{OFF}

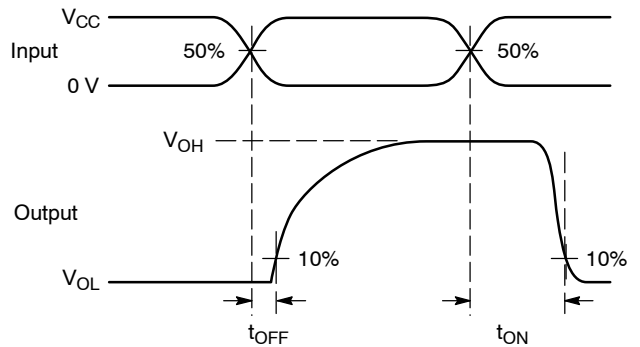
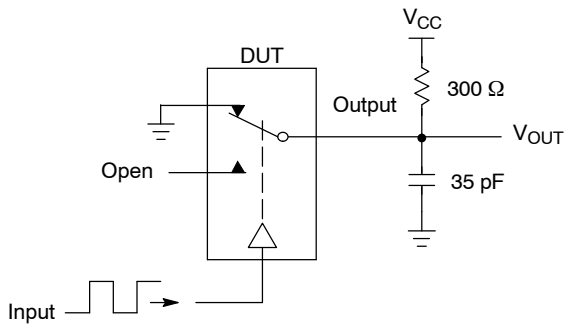
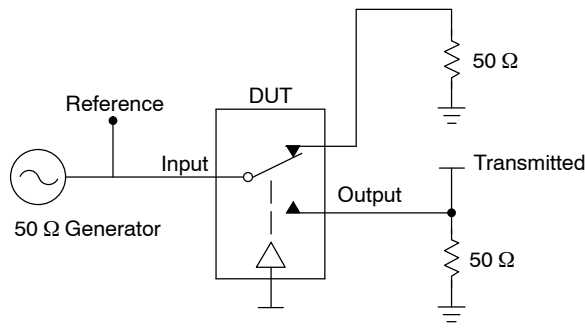


Figure 6. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

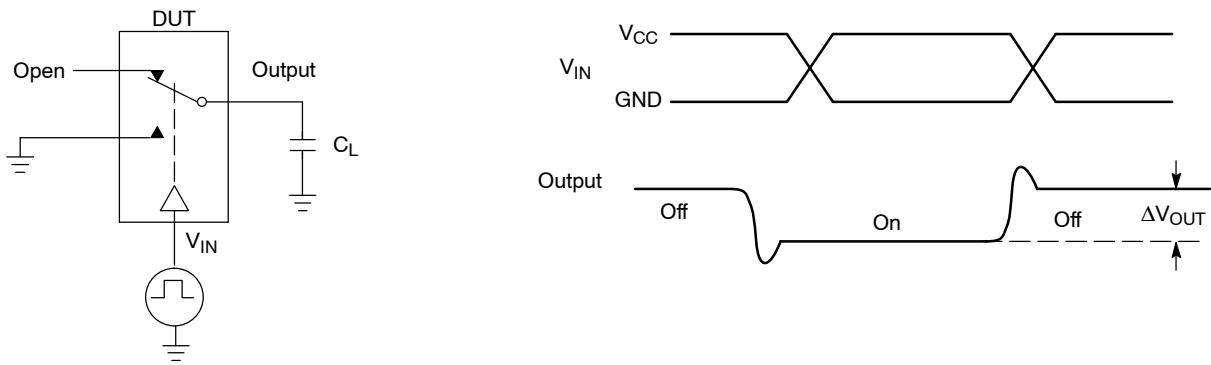


Figure 8. Charge Injection: (Q)

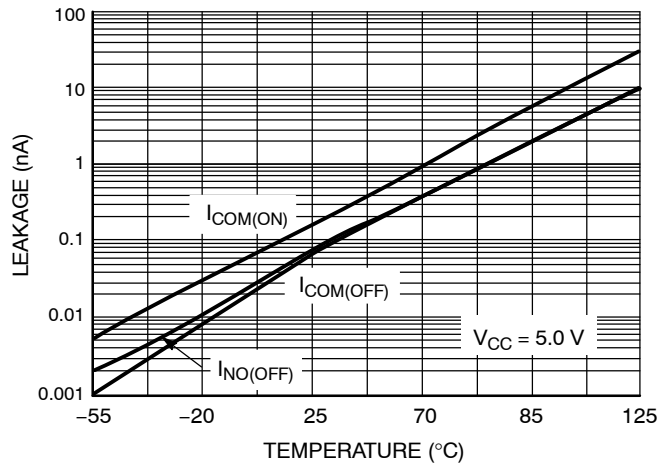


Figure 9. Switch Leakage vs. Temperature

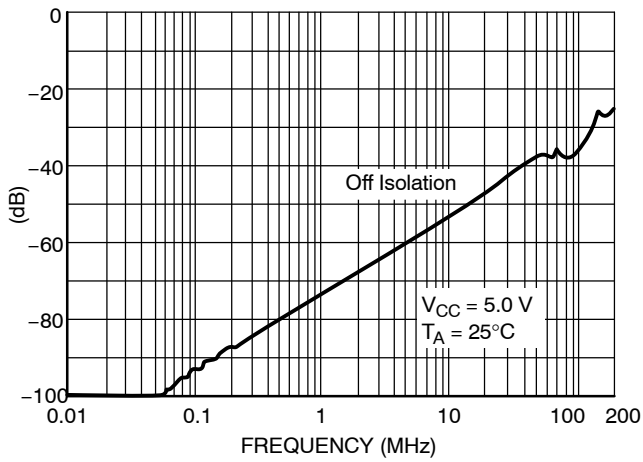


Figure 10. Off-Channel Isolation

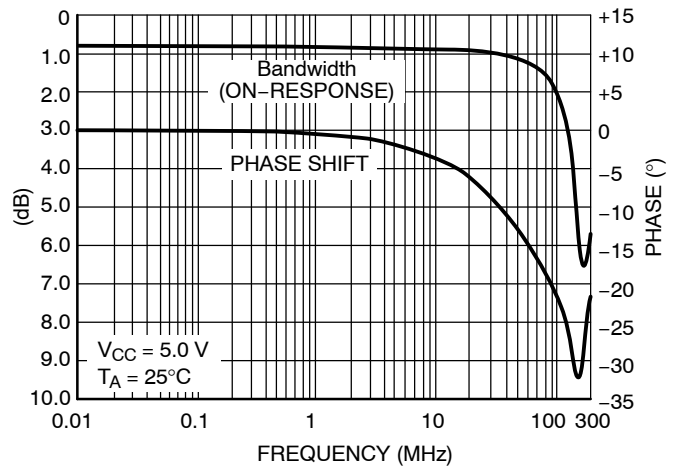


Figure 11. Typical Bandwidth and Phase Shift

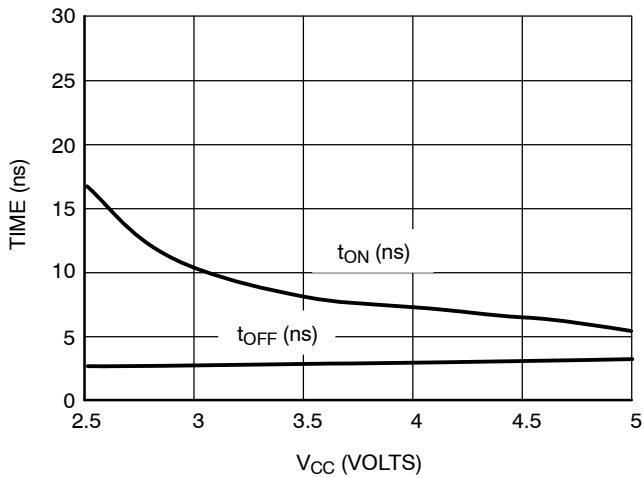


Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25°C

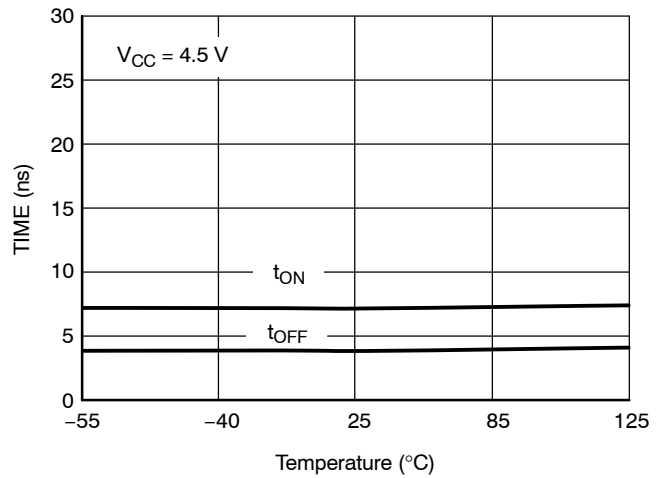


Figure 13. t_{ON} and t_{OFF} vs. Temp

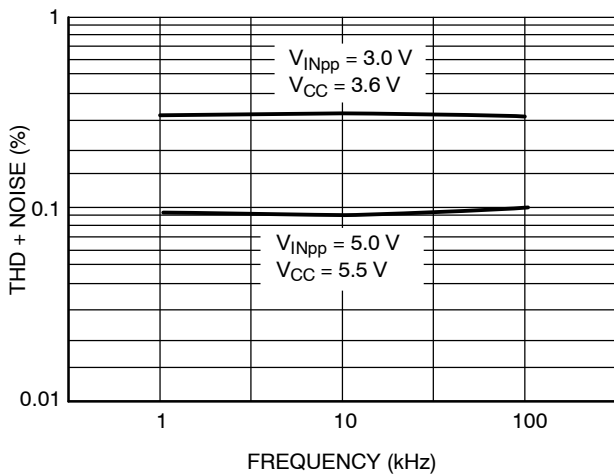


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

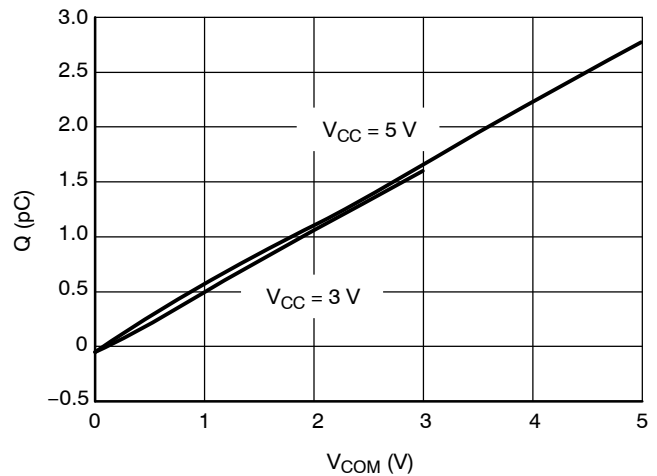


Figure 15. Charge Injection vs. COM Voltage

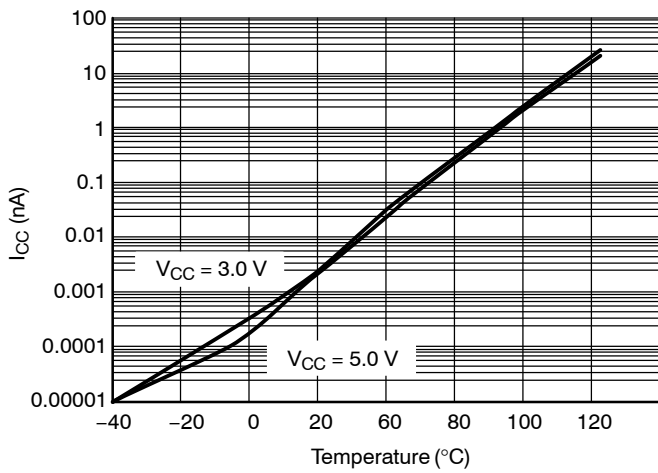


Figure 16. I_{CC} vs. Temp, $V_{CC} = 3\text{ V}$ and 5 V

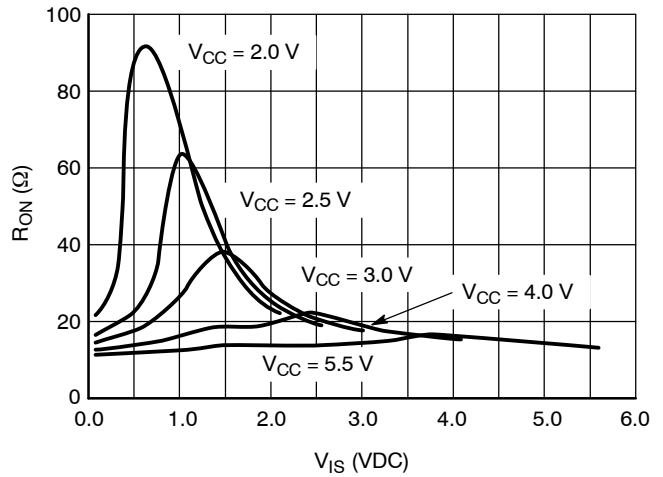


Figure 17. R_{ON} vs. V_{CC} , Temp = 25°C

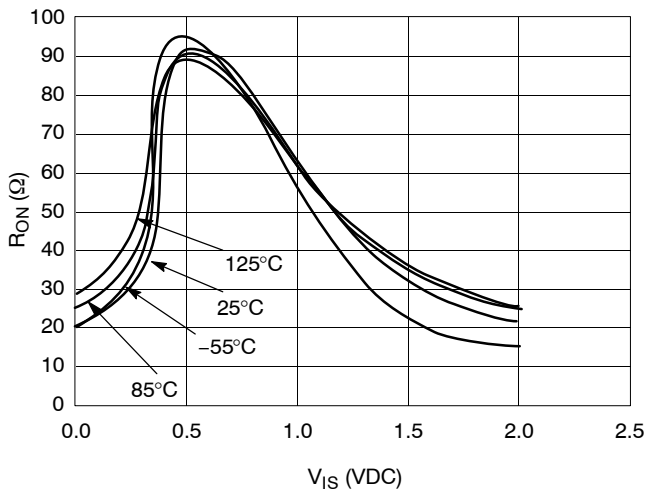


Figure 18. R_{ON} vs Temp, $V_{CC} = 2.0\text{ V}$

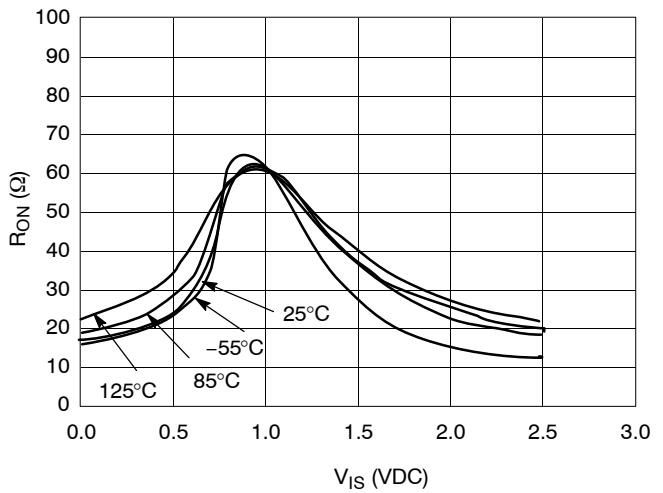


Figure 19. R_{ON} vs. Temp, $V_{CC} = 2.5\text{ V}$

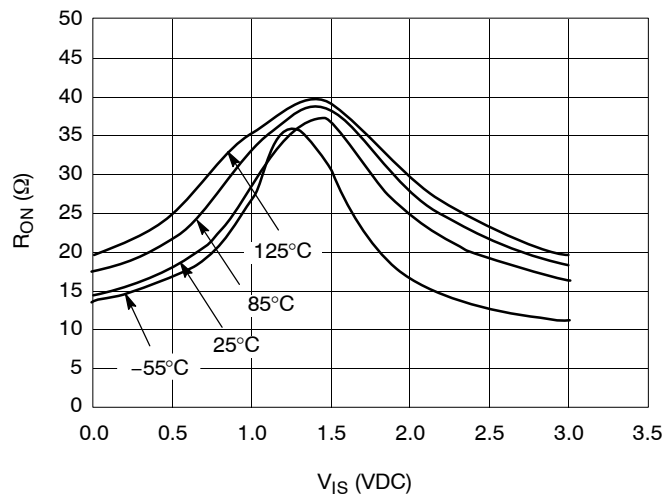


Figure 20. R_{ON} vs. Temp, $V_{CC} = 3.0\text{ V}$

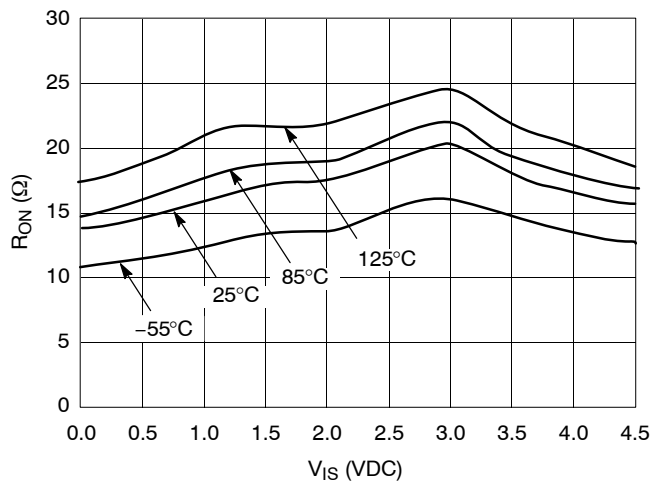


Figure 21. R_{ON} vs. Temp, $V_{CC} = 4.5\text{ V}$

NLAST44599

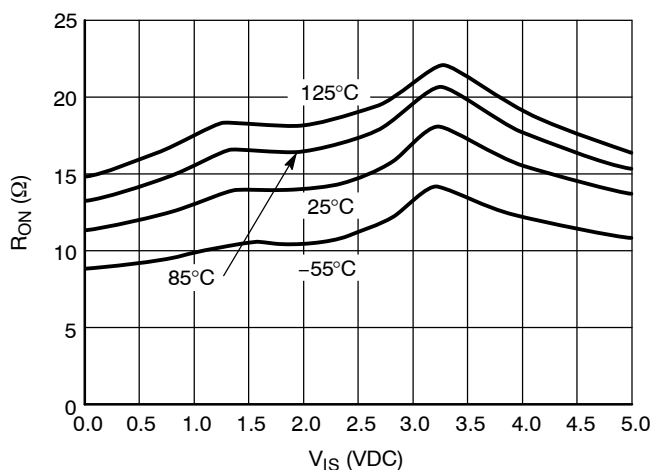


Figure 22. R_{ON} vs. Temp, $V_{CC} = 5.0$ V

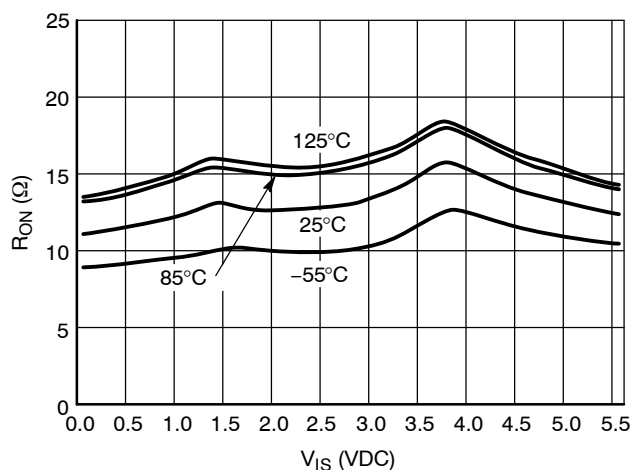


Figure 23. R_{ON} vs. Temp, $V_{CC} = 5.5$ V

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature					Package Type	Shipping [†]
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NLAST44599DT	NL	AS	44599	DT		TSSOP-16*	96 Unit / Rail
NLAST44599DTR2	NL	AS	44599	DT	R2	TSSOP-16*	2500 / Tape & Reel
NLAST44599MN	NL	AS	44599	MN		QFN-16	124 Unit Rail
NLAST44599MNG	NL	AS	44599	MN		QFN-16 (Pb-Free)	124 Unit Rail
NLAST44599MNR2	NL	AS	44599	MN	R2	QFN-16	2500 / Tape & Reel
NLAST44599MNR2G	NL	AS	44599	MN	R2	QFN-16 (Pb-Free)	2500 / Tape & Reel

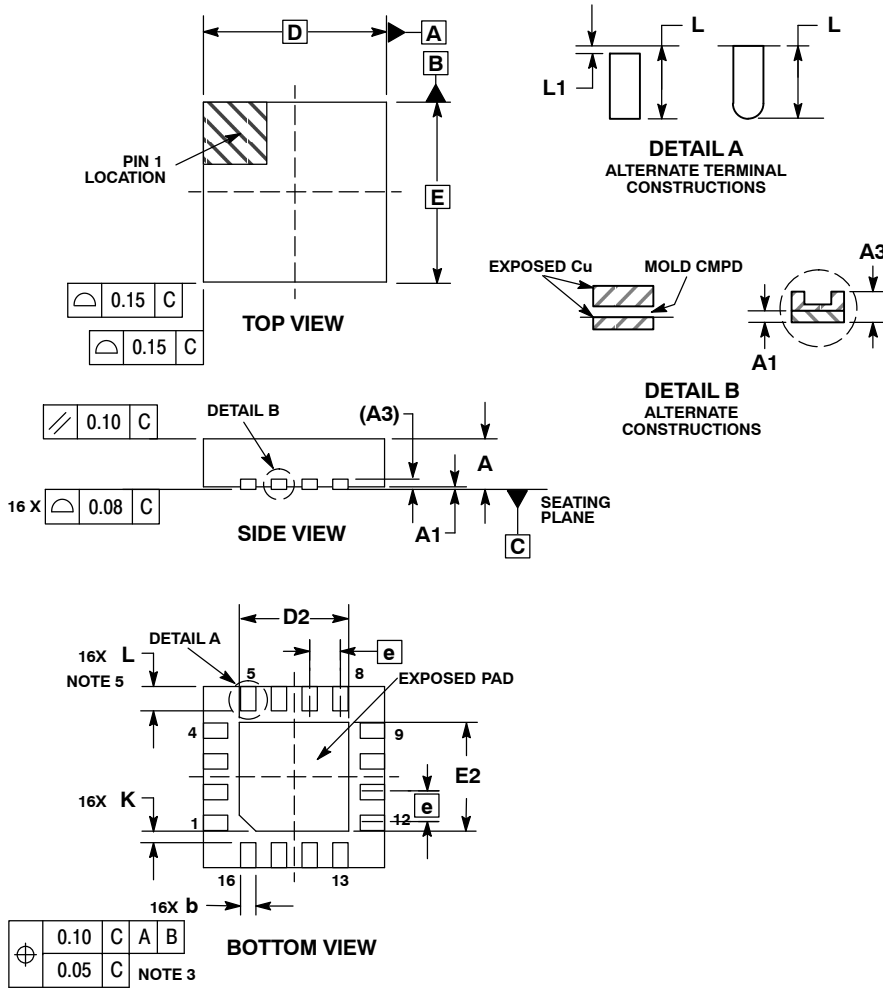
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

NLAST44599

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G-01
ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

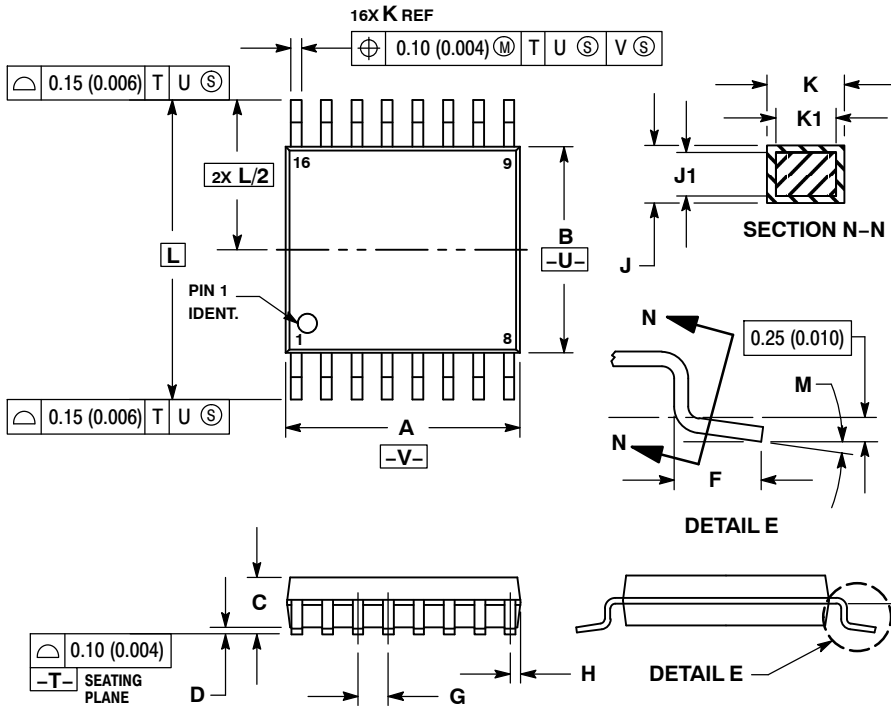
DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
<i>b</i>	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
<i>e</i>	0.50	BSC
K	0.18	TYP
L	0.30	0.50
L1	0.00	0.15

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F-01
ISSUE B

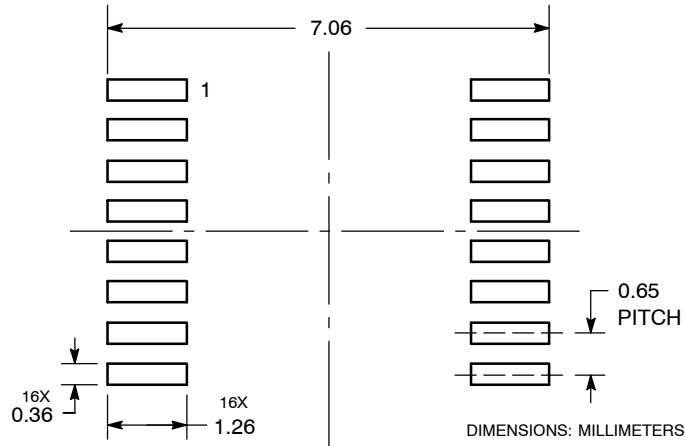
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative